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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,219	09/24/2003	Masaaki Nishijima	10873.1307US01	2145

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EXAMINER	
HA, NATHAN W	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 01/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,219	NISHIJIMA ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Cancellation of claims 2-3 is acknowledged.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichikawa (US 5,905,301, previously cited) and in view of Gibson (US 6,621,140, previously cited.)

In regard to claims 1 and 9, the seventh embodiment of the device disclosed in Ichikawa, depicted in figs. 11 (a) and (b), discloses a semiconductor device that anticipates all the points of claim 1. The device includes a mold resin (75) sealing a semiconductor chip (74), a plurality of conductor leads (72) with internal and external terminal portions relative to the mold resin, a conductor lead being connected to an electrode of the semiconductor chip, and at least one conductor lead whose internal terminal portion forms an inductance element portion, at least a part of which is narrower than the external terminal portion. (Note that in the 'Background of the Invention' section Ichikawa discloses that

leads have "inductance components," and thus constitute inductance element portions.)

The seventh embodiment of the device disclosed in Ichikawa, depicted in figs. 11 (a) and (b), further discloses a semiconductor device where the conductor lead having the inductance element portion (72) has an overlapping portion overlapping a lower surface of the semiconductor chip (74) and is connected to the semiconductor chip in the overlapping portion (in this case, via a plurality of projection electrodes (77) which are formed on an electrode formation surface of the chip (74)). 7.

Ichikawa, however, does not describe a device where the inductance element portion has a meandering planar shape.

Gibson discloses an analogous device that integrates an inductor into a semiconductor package by integrally forming inductive segments in the leadframe, and notes in the abstract that the inductance values may be controlled by the shape and size of the inductive segments. Furthermore, figs. 2,5 and 6 in Gibson clearly show examples of inductive element portions of the leadframe that have a plurality of alternate shapes (including a meandering planar shape, as depicted in fig. 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to alter the shape of the inductive element portions of the semiconductor device as appropriate for the aim of controlling the inductance values and achieving stable inductance characteristics.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ichikawa and Gibson as applied to claims 1 and 9 above, and further in view of Ohmuro US 5,994,763, previously cited.

The combination of Ichikawa and Gibson describes a semiconductor packaging device that discloses all the points of claims 1 and 9, but does not describe a device where the semiconductor chip and the overlapping portion of the conductor lead are reconnected via an electrical conductor in a via hole formed in the semiconductor chip, as described in claim 4.

Ohmuro discloses a device with electrical conductors in via holes formed in a semiconductor chip. Specifically, Ohmuro discloses a wiring structure that electrically connects the backside surface of the semiconductor (specifically, the backside wiring grove) to the front surface of the semiconductor chip (specifically, the surface electrodes).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the electrodes of the semiconductor chip to the leads that overlap the lower portion of the semiconductor chip through the means of via holes in the semiconductor chip (as opposed to using a plurality of projection electrodes, for example, as in Ichikawa) in the interests of minimizing space and eliminating the need for inductance element portions, such as bonding wires, that have unstable inductance characteristics. 9.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ichikawa and Gibson as applied to claims 1 and 9 above, and further in view of Efland et al. US 6,140,702, previously cited, hereinafter, Efland.

The combination of Ichikawa and Gibson describes a semiconductor packaging device that discloses all the points of claims 1 and 9, but does not describe a device where the overlapping portion of the conductor lead forms a die pad portion on which the semiconductor chip is mounted, as described in claim 5.

It is well known in the art that segments of the leadframe can form die pad portions on which the die and semiconductor chip can be mounted. For example, in Efland's discussion of prior art, fig, 1 clearly shows a semiconductor packaging device that includes a lead frame, a portion of which will overlap the lower surface of the semiconductor chip, and which constitutes the die pad portion on which the die and chip is mounted.

Note that, in figs. 1(a) and (b), Ichikawa discloses a semiconductor chip mounted on an overlapping portion of the conductor lead frame, although omits disclosing how it is mounted. However, in view of Efland, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a die pad portion on this segment of the conductor lead frame that overlaps the lower surface of the semiconductor chip, to enable the chip to be mounted on that segment. 10.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ichikawa as applied to claims 1 and 9 above, and further in view of Fithian et al. US 4,967,258, previously cited, hereinafter, Fithian.

Ichikawa describes a semiconductor packaging device that discloses all the points of claim 1, but does not describe a device where the conductor lead

having the inductance element portion is connected to a source of a field effect transistor (FET), as described in claim 6, or a gate or drain of a FET, as described in claim 7.

Fithian discloses a package for housing a FET device. It is well known in the art that a FET has three terminals: a gate, a drain and a source. Fithian's device, as depicted in figs. 2 5, clearly displays a package housing an FET chip with protruding gate, drain and source conductor leads constituting the interface to the FET and connected to the appropriate terminals of the FET.

Therefore, if an FET is formed in the semiconductor chip, it would have been obvious to one of ordinary skill in the art at the time the invention was made to connect a conductor lead to the source terminal of the FET (in the case of claim 6) or to the gate or drain terminals of the FET (in the case of claim 7), in order for that FET to function as necessary. 11.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ichikawa as applied to claims 1 and 9 above, and further in view of Dobrovolny et al. US 3,909,726, previously cited, hereinafter, Dobrovolny.

Ichikawa describes a semiconductor packaging device that discloses all the points of claim 1, but does not describe a device where a conductor lead functions as a choke inductor, as described in claim 8.

Dobrovolny discloses an electrical device where a conductor lead functions as a choke inductor. Specifically, figs. 2(a) and (b) clearly depict inductors L6, L12, L13, L14, L18 which function as wire wound radio frequency chokes. Each inductor has two lead ends connected to exposed conductive

segments of the conductive layers of the device. Thus, these conductor leads constitute choke inductors.

Therefore, if would have been obvious to one of ordinary skill in the art at the time the invention was made to allow one of the conductor leads to function as a choke inductor, if doing so would obviously facilitate the efficient operation, and meet the design criteria, of the semiconductor device.

Response to Arguments

3. Applicant's arguments filed 11/15/04 have been fully considered but they are not persuasive. For instance, Applicants contend that the cited art does not disclose a semiconductor device wherein a chip is mounted on and connected to the inductance elements of a conductor lead. This limitation can be found in Ichikawa's fig. 11b, wherein the leads are connected to the chip through elements 77.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory

action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
January 19, 2005

HOAI PHAM
PRIMARY EXAMINER